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# AKD4114-B

## AK4114 Evaluation Board Rev.0

## GENERAL DESCRIPTION

AKD4114-B is the evaluation board for AK4114, 192kHz digital audio transceiver. This board has optical and BNC connector to interface with other digital audio equipment.

### ■ Ordering guide

AKD4114-B --- Evaluation board for AK4114
(A cable for connecting with printer port of IBM-AT compatible PC and a control software are packed with this. The control software does not operate on Windows NT.)

## FUNCTION

**□ Digital interface**

**-S/PDIF :**
**8 channel input (optical or BNC)**
**2 channel output (optical or BNC )**

**- Serial audio data I/F :**
**1 input/output (for DIR deta output/DIT data input. 10-pin port)**

**-B,C,U,V bit :**
**1 input/output port (10-pin port)**

**-Serial control data I/F**
**1 input/output port (10-pin port)**

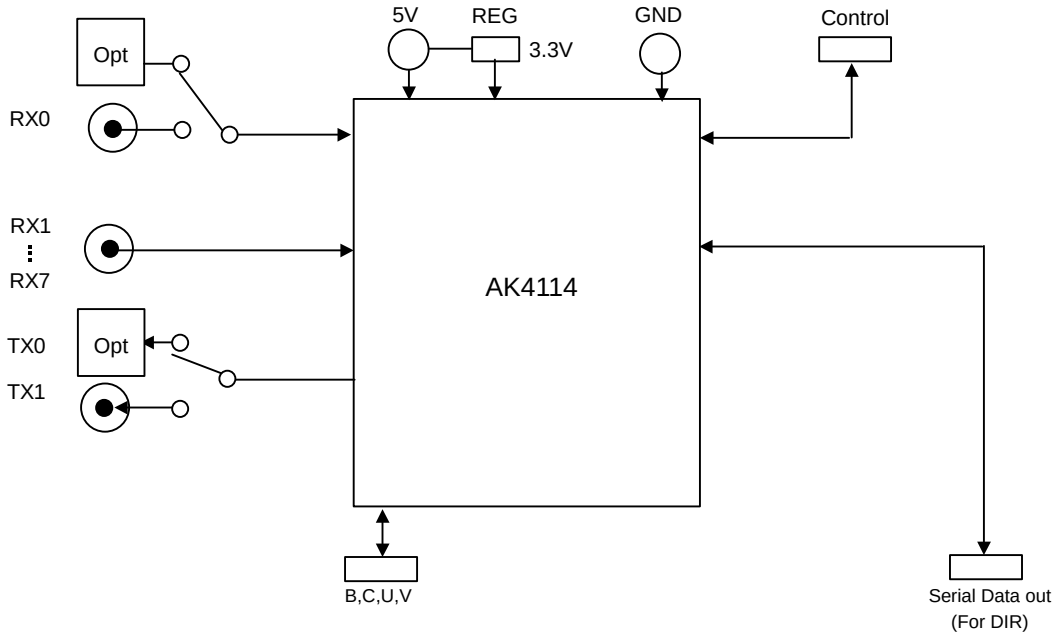



Figure 1. AKD4114-B Block Diagram
*Circuit diagram and PCB layout are attached at the end of this manual.

# Evaluation Board Manual

## ■ Operating sequence

(1) **Set up the power supply lines.**
[+ 5V] (Red) = 5V
[GND] (Black) = 0V

Each supply line should be distributed from the power supply unit.

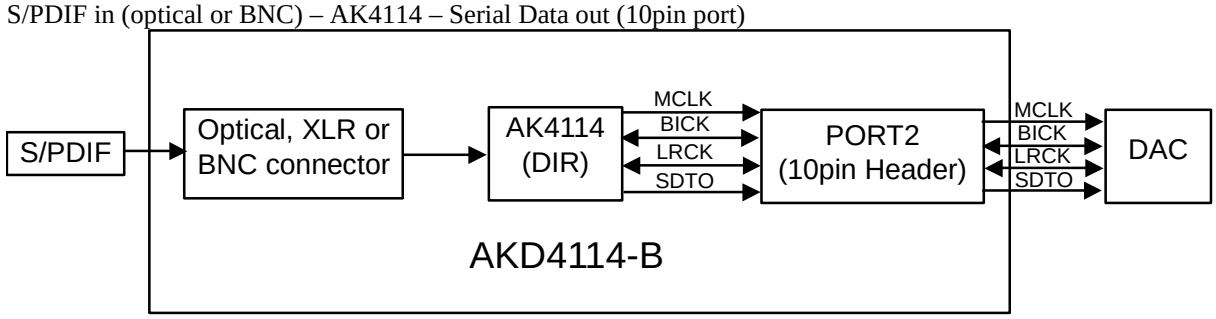
(2) **Set up the evaluation mode and jumper pins.** (Refer to the following item.)

(3) **Connect cables.** (Refer to the following item.)

(4) **Power on.**
The AK4114 should be reset once bringing PDN(SW2) "L" upon power-up.

## ■ Evaluation modes

(1) Evaluation for DIR (Default)
S/PDIF in (optical or BNC) – AK4114 – Serial Data out (10pin port)




The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector(PORT1: TORX176) or BNC connector. The AKD4114-B can be connected with the AKM's DAC evaluation board via 10-line cable.

a. Set-up of Bi-phase Input

RX0 and RX1-7 should not select BNC at the same time.

a-1. RX0

| Connector | JP2(RXP0) | JP3(RXN0) |
|---|---|---|
| Optical (PORT1) | OPT | BNC |
| BNC (J2) | BNC | BNC |

Table 1. Set-up of RX0

a-2. RX1, 2, 3, 4, 5, 6, and 7 can be inputted from a BNC (J2) connector only.
Only RX1, RX2 and RX 3 can be used in parallel mode. The jumper which selects the Rx channel should be Short.

| Input | RX1 | RX2 | RX3 | RX4 | RX5 | RX6 | RX7 |
|---|---|---|---|---|---|---|---|
| JP | JP4 | JP5 | JP6 | JP7 | JP8 | JP9 | JP10 |
| | Short | Short | Short | RX4 | RX5 | RX6 | RX7 |

Table 2. Set-up of RX1, 2, 3, 4, 5, 6 and 7

a-3. Set-up of AK4114 input path

It sets up by SW 1_1 and SW 1_5 in parallel mode. Please set up IPS2-0 bits in serial mode.

| - | IPS1 pin (SW1_5) | IPS0 pin (SW1_1) | INPUT Data | |
|---|---|---|---|---|
| IPS2 bit | IPS1 bit | IPS0 bit | | |
| 0 | 0 | 0 | RX0 | Default |
| 0 | 0 | 1 | RX1 | |
| 0 | 1 | 0 | RX2 | |
| 0 | 1 | 1 | RX3 | |
| 1 | 0 | 0 | RX4 | |
| 1 | 0 | 1 | RX5 | |
| 1 | 1 | 0 | RX6 | |
| 1 | 1 | 1 | RX7 | |

(In parallel mode, IPS2 is fixed to "0")

Table 3. Recovery Data Select

b. Set-up of clock input and output

The signal level outputted/inputted from PORT2 is 3.3V.

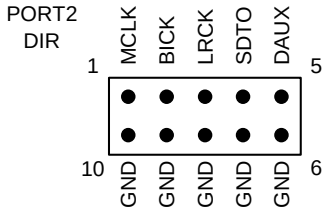



Figure 2. PORT2 pin layout

b-1. MCKO1/MCKO2

The output of MCKO1 pin or MCKO2 pin can be selected by JP12. The output frequency of MCKO1/MCKO2 is selected by OCKS 1-0.

| Output signal | JP12 | |
|---|---|---|
| MCKO1 | MCKO1 | Default |
| MCKO2 | MCKO2 | |

Table 4. Set-up of MCKO1/MCKO2

| OCKS1 pin (SW3_2) | OCKS0 pin (SW3_3) | (X'tal) | MCKO1 | MCKO2 | fs (max) | |
|---|---|---|---|---|---|---|
| OCKS1 bit | OCKS0 bit | | | | | |
| 0 | 0 | 256fs | 256fs | 256fs | 96 kHz | Default |
| 0 | 1 | 256fs | 256fs | 128fs | 96 kHz | |
| 1 | 0 | 512fs | 512fs | 256fs | 48 kHz | |
| 1 | 1 | 128fs | 128fs | 64fs | 192 kHz | |

Table 5. Master Clock Frequency Select

b-2. Set-up of input/output of BICK and LRCK

Please select SW 3_7 (DIR_I/O) according to the setup of audio format of AK4114 (Refer to Table 7).

| Audio format | SW3_7 (DIR_I/O) | |
|---|---|---|
| Slave mode | 0 | Default |
| Master mode | 1 | |

Table 6. Set-up of DIR_I/O

c. Set-up of Audio format

It sets up by SW 1_2, SW 1_3 and SW1_4 in parallel mode. Please set up DIF2-0 bit in serial mode.

| Mode | DIF2 pin (SW1_4) | DIF1 pin (SW1_3) | DIF0 pin (SW1_2) | DAUX | SDTO | LRCK | | BICK | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | DIF2 bit | DIF1 bit | DIF0 bit | | | | I/O | | I/O | |
| 0 | 0 | 0 | 0 | 24bit, Left justified | 16bit, Right justified | H/L | O | 64fs | O | |
| 1 | 0 | 0 | 1 | 24bit, Left justified | 18bit, Right justified | H/L | O | 64fs | O | |
| 2 | 0 | 1 | 0 | 24bit, Left justified | 20bit, Right justified | H/L | O | 64fs | O | |
| 3 | 0 | 1 | 1 | 24bit, Left justified | 24bit, Right justified | H/L | O | 64fs | O | |
| 4 | 1 | 0 | 0 | 24bit, Left justified | 24bit, Left justified | H/L | O | 64fs | O | |
| 5 | 1 | 0 | 1 | 24bit, $I^2S$ | 24bit, $I^2S$ | L/H | O | 64fs | O | |
| 6 | 1 | 1 | 0 | 24bit, Left justified | 24bit, Left justified | H/L | I | 64-128fs | I | Default |
| 7 | 1 | 1 | 1 | 24bit, $I^2S$ | 24bit, $I^2S$ | L/H | I | 64-128fs | I | |

Table 7. Audio format

d. Set-up of CM1 and CM0

The operation mode of PLL is selected by CM1 and CM0. In parallel mode, it can be selected by SW3_1 and JP18. In serial mode, it can be selected by CM1-0 bits.

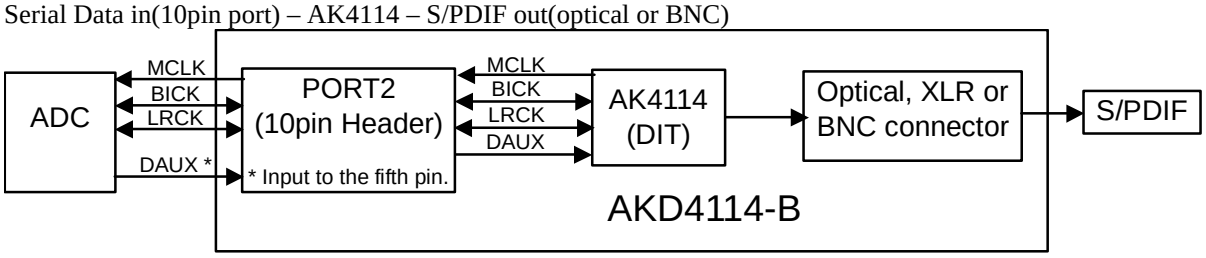
| CM1 pin (SW3_1) | CM0 pin (JP18) | (UNLOCK) | PLL | X'tal | Clock source | SDTO source | |
|---|---|---|---|---|---|---|---|
| CM1 bit | CM0 bit | | | | | | |
| 0 | 0 (CM0) | - | ON | ON(Note) | PLL(RX) | RX | Default |
| 0 | 1 (CDTO/CM0=H) | - | OFF | ON | X'tal | DAUX | |
| 1 | 0 (CM0) | 0 | ON | ON | PLL(RX) | RX | |
| | | 1 | ON | ON | X'tal | DAUX | |
| 1 | 1 (CDTO/CM0=H) | - | ON | ON | X'tal | DAUX | |

ON: Oscillation (Power-up), OFF: STOP (Power-Down)

Note: When the X'tal is not used as clock comparison for fs detection (XTL0, 1= "1,1"), the X'tal is OFF.

Table 8. Clock Operation Mode Select

(2) Evaluation for DIT
Serial Data in(10pin port) – AK4114 – S/PDIF out(optical or BNC)




MCLK, BICK, LRCK and DAUX are input the via 10pin header (PORT2: DIR).

a. Set-up of a Bi-phase output signal

TX0 and TX1 should not select an optical connector or a BNC connector at the same time.

a-1. The data outputted from TX1 can be selected by OPS12-10 bit.

| Connector | JP19 (TX1) | JP14 (TX1) |
|---|---|---|
| Optical (PORT4) | OPT | BNC |
| BNC (J4) | BNC | BNC |

Table 9. Set-up of TX1

a-2. As for TX0, only the loop back mode of RX corresponds. This mode is fixed to RX0 in parallel mode. In serial mode, it can be selected by OPS02-00 bits.

| Connector | JP13 (TX0) | JP19 (TXP1) | JP14 (TXN1) |
|---|---|---|---|
| Optical (PORT4) | OPT | Open | BNC |
| BNC (J4) | BNC | Open | BNC |

Table 10. Set-up of TX0

b. Set-up of clock input and output

The used signals are MCLK, LRCK, BICK, and DAUX.
The signal level outputted and inputted from PORT2 is 3.3V.

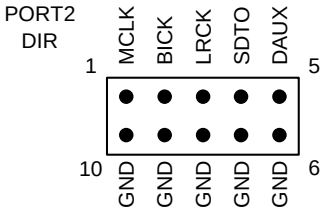



Figure 3. PORT2 pin layout

| Clock | PORT | I/O |
|---|---|---|
| MCLK | PORT2 | OUT |
| BICK | PORT2 | IN / OUT |
| LRCK | PORT2 | IN / OUT |
| DAUX | PORT2 | IN |

Table 11. Clock input/output

b-1. MCKO1/MCKO2

The output of MCKO1 pin or MCKO2 pin can be selected by JP12. The output frequency of MCKO1/MCKO2 sets up by OCKS 1-0.

| Output signal | JP12 | |
|---|---|---|
| MCKO1 | MCKO1 | Default |
| MCKO2 | MCKO2 | |

Table 12. Selection of MCKO1/MCKO2

| OCKS1 pin (SW3_2) / OCKS1 bit | OCKS0 pin (SW3_3) / OCKS0 bit | (X'tal) | MCKO1 | MCKO2 | fs (max) | |
|---|---|---|---|---|---|---|
| 0 | 0 | 256fs | 256fs | 256fs | 96 kHz | Default |
| 0 | 1 | 256fs | 256fs | 128fs | 96 kHz | |
| 1 | 0 | 512fs | 512fs | 256fs | 48 kHz | |
| 1 | 1 | 128fs | 128fs | 64fs | 192 kHz | |

Table 13. Master Clock Frequency Select

b-2. Set-up of input/output of BICK and LRCK

Please set up SW 3_8 (DIT_I/O) according to the setup of audio format of AK4114 (Refer to Table 20). JP16 and 17 should be fixed to the "DC" side.

| Audio format | SW3_8 (DIT_I/O) | |
|---|---|---|
| Slave mode | 0 | Default |
| Master mode | 1 | |

Table 14. Set-up of DIT_I/O

c. Set-up of audio data format

Please refer to Table 7.

d. Set-up of CM1 and CM0

| CM1 pin (SW3_1) / CM1 bit | CM0 pin (JP18) / CM0 bit | (UNLOCK) | PLL | X'tal | Clock source | SDTO source | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | - | ON | ON(Note) | PLL(RX) | RX | Default |
| 0 | 1 | - | OFF | ON | X'tal | DAUX | |
| 1 | 0 | 0 | ON | ON | PLL(RX) | RX | |
| | | 1 | ON | ON | X'tal | DAUX | |
| 1 | 1 | - | ON | ON | X'tal | DAUX | |

ON: Oscillation (Power-up), OFF: STOP (Power-Down)
Note: When the X'tal is not used as clock comparison for fs detection (XTL0, 1= "1,1"), the X'tal is OFF.
Table 15. Clock Operation Mode Select

## ■ B, C, U, V Inputs and output

B(block start), C(channel status), U(user data) and V(validity) are inputted/outputted via 10pin header (PORT3: BCUV). Pin arrangement of PORT3 has become like Figure 3.

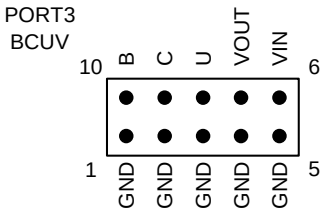



Figure 4. PORT3 pin layout

## ■ Serial control

The AK4114 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT6 (uP-I/F) with PC by 10-line flat cable packed with the AKD4114-B. Take care of the direction of connector. There is a mark at pin#1. The pin layout of PORT6 is as Figure 5.

| Mode | SW1_6 | JP18 |
|---|---|---|
| 4 wire Serial | L | CDTO/CM0="H" |
| IIC | H | SDA and CM0="L"(Note) |

Note: In IIC mode, the chip address is fixed to "01".
Table 16. Set-up of Parallel mode and Serial mode

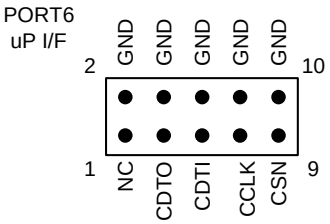



Figure 5. PORT6 pin layout

This evaluation board encloses control software. A software operation procedure is included in an evaluation board manual.

■ **Toggle switch set-up**

| | | |
|---|---|---|
| SW2 | PDN | Reset switch for AK4114. Set to "H" during normal operation. Bring to "L" once after the power is supplied. |

■ **LED indication**

| | | |
|---|---|---|
| LE1 | INT0 | Bright when INT0 pin goes to "H". |
| LE2 | INT1 | Bright when INT1 pin goes to "H". |

■ **DIP switch (SW1) set-up: -off- means "L"**

| No. | Switch Name | Function | Default |
|---|---|---|---|
| 1 | IPS0 | Set-up of IPS0 pin. (in parallel mode) | OFF |
| 2 | DIF0 | Set-up of DIF0 pin. (in parallel mode) | OFF |
| 3 | DIF1 | Set-up of DIF1 pin. (in parallel mode) | ON |
| 4 | DIF2 | Set-up of DIF2 pin. (in parallel mode) | ON |
| 5 | IPS1/IIC | Set-up of IPS1 pin. (in parallel mode)<br>Set-up of IIC pin. (in serial mode) "L": 4 wire Serial, "H": IIC | OFF |
| 6 | P/SN | Set-up of P/SN pin. "L": Serial mode, "H": Parallel mode | OFF |
| 7 | TEST | Don't care | OFF |
| 8 | ACKS | Don't care | OFF |

■ **DIP switch (SW3) set-up: -off- means "L"**

| No. | Switch Name | Function | Default |
|---|---|---|---|
| 1 | CM1 | Set-up of CM1 pin. (in parallel mode) | OFF |
| 2 | OCKS1 | Set-up of OCKS1 pin. (in parallel mode) | OFF |
| 3 | OCKS0 | Set-up of OCKS0 pin. (in parallel mode) | OFF |
| 4 | PSEL | Don't care | OFF |
| 5 | XTL0 | See Table 17 | OFF |
| 6 | XTL1 | | OFF |
| 7 | DIR_I/O | Set-up of the transmission direction of 74AC245<br>"L": When inputting from PORT2, "H": When outputting from PORT2 | ON |
| 8 | DIT_I/O | Don't care | OFF |

■ **Set-up of XTL1 and XTL0**

| SW3_6 | SW3_5 | X'tal Frequency | |
|---|---|---|---|
| XTL1 | XTL0 | X'tal | |
| 0 | 0 | 11.2896MHz | Default |
| 0 | 1 | 12.288MHz | |
| 1 | 0 | 24.576MHz | |
| 1 | 1 | (Use channel status) | |

Table 17. Set-up of XTL1 and XTL0

■ **Jumper set up.**

| No. | Jumper Name | Function |
|---|---|---|
| 1 | D3V/VD | Set-up of Power supply source for 74AC245.<br>D3V : D3V (default)<br>VD : VD |
| 2 | RXP0 | Set-up of RXP0 input circuit.<br>OPT : Optical (default)<br>BNC : BNC |
| 4,5,6 | RX1-3 | Set-up of RX1-3 input circuit. |
| 7,8,9,10 | RX4-7 | RX4-7 set-up depending serial/parallel mode<br>RX4-7 : Serial mode (default)<br>DIF2-0,IPS0 : Parallel mode |
| 11,12 | DIR MCLK ,<br>DIT MCLK | MCKO set-up for PORT5(DIT) and PORT2(DIR)<br>MCKO1 : MCKO1 of AK4114 (default)<br>MCKO2 : MCKO2 of AK4114 |
| 13 | TX0 | Set-up of TX0 output circuit.<br>OPT : Optical<br>BNC : BNC (default) |
| 18 | SDA/CDTO | Set-up of SDA/CDTO pin.<br>4 wire Serial : CDTO/CM0="H". (default)<br>IIC : SDA |
| 19 | TXP1 | Set-up of TXP1 input circuit.<br>OPT : Optical (default)<br>BNC : BNC |

# Control Software Manual

## ■ Set-up of evaluation board and control software

1. Set up the AKD4114-B according to previous term.

2. Connect IBM-AT compatible PC with AKD4114-B by 10-line type flat cable (packed with AKD4114-B). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AKD4114-B Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “akd4114-b0.exe” to set up the control program.

5. Then please evaluate according to the follows.

## ■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Write default” button.
3. Then set up the dialog and input data.

## ■ Explanation of each buttons

1. [Port Setup] : Set up the printer port.
2. [Write default] : Initialize the register of AK4114.
3. [All Write] : Write all registers that is currently displayed.
4. [Read All] : All the registers of AK4114 are read.
5. [Function1] : Dialog to write data by keyboard operation.
6. [F3] : Dialog of sequential writing.
7. [SAVE] : Save the current register setting.
8. [OPEN] : Write the saved values to all register.
9. [Write] : Dialog to write data by mouse operation.
10. [Read] : The data corresponding to each register is read.

## ■ Explanation of each dialog

1. [Function1 Dialog] : Dialog to write data by keyboard operation

   Address Box: Input register address in 2 figures of hexadecimal.
   Data Box: Input register data in 2 figures of hexadecimal.

   If you want to write the input data to AK4114, click “OK” button. If not, click “Cancel” button.

2. [Write Dialog] : Dialog to write data by mouse operation

   There are dialogs corresponding to each register.

   Click the “Write” button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

   If you want to write the input data to AK4114, click “OK” button. If not, click “Cancel” button.

## ■ Indication of data

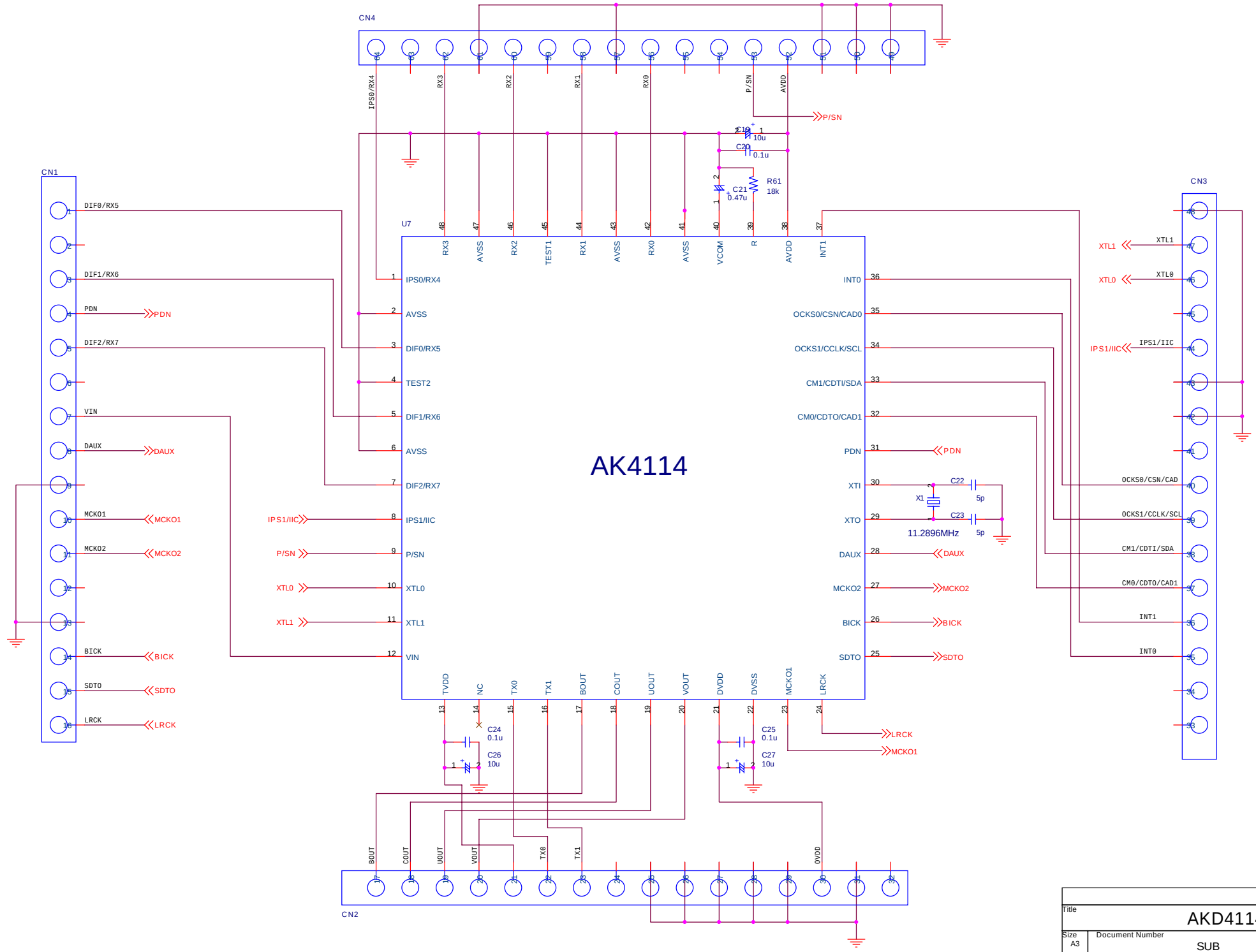
Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

## ■ Attention on the operation

If you set up Function1 dialog, input data to all boxes. Attention dialog is indicated if you input data or address that is not specified in the datasheet or you click “OK” button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click “Cancel” button or check the check box.

## REVISION HISTORY

| Date (yy/mm/dd) | Manual Revision | Board Revision | Reason | Page | Contents |
|---|---|---|---|---|---|
| 04/11/22 | KM076600 | 0 | First edition | | |
| 05/06/21 | KN076601 | 0 | Change | 13-15 | Circuit diagram was changed |
| 05/12/22 | KM076602 | 0 | Addition | 2,5 | Block diagram at DIR/DIT Evaluation was added. |
| 07/12/19 | KM076603 | 0 | Modification | 5 | DIT Evaluation item was modified. |

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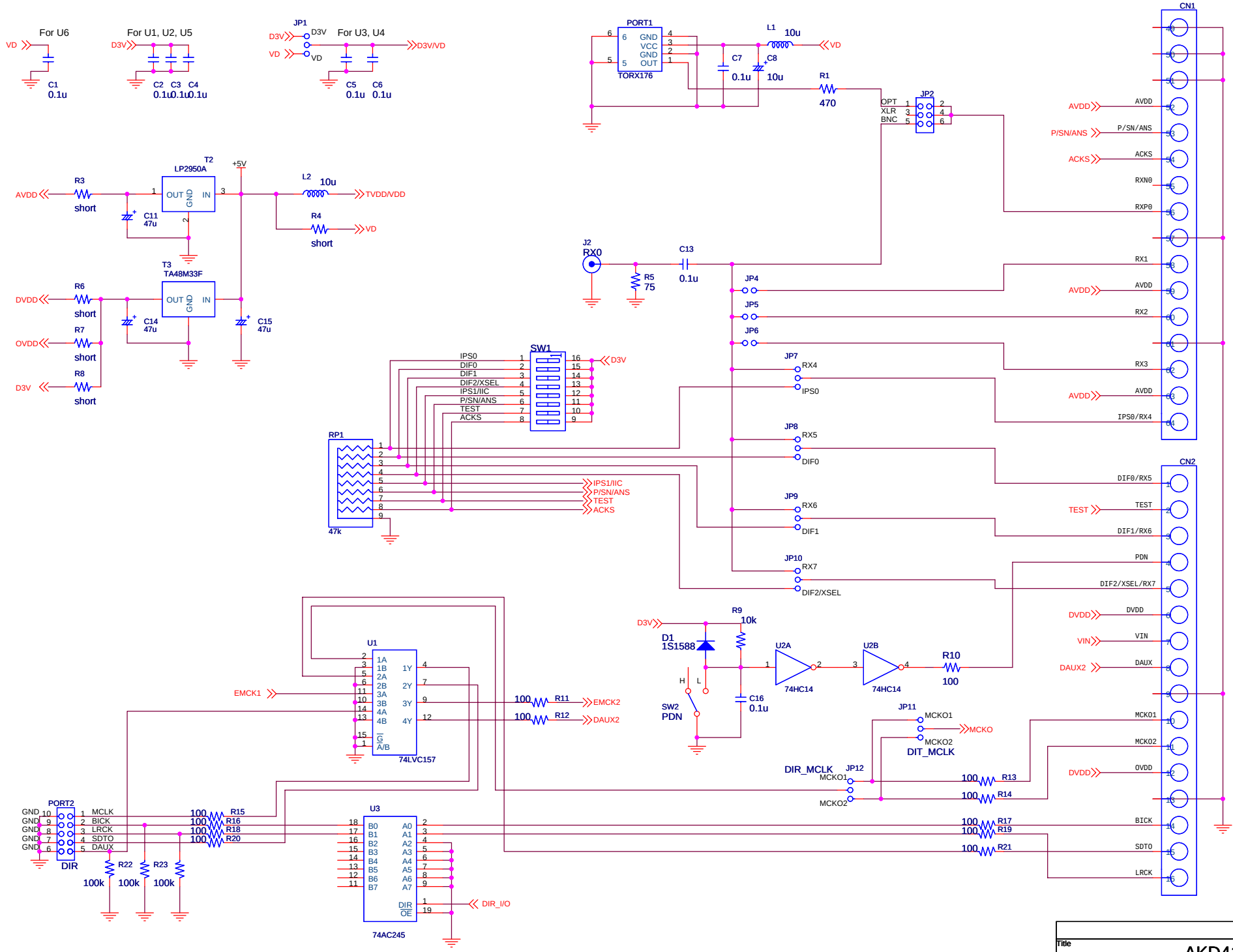
|---|---|---|
| Title | AKD4114 | |
| Size A3 | Document Number SUB | Rev A |
| Date: Monday, November 22, 2004 | Sheet 3 of 3 | |

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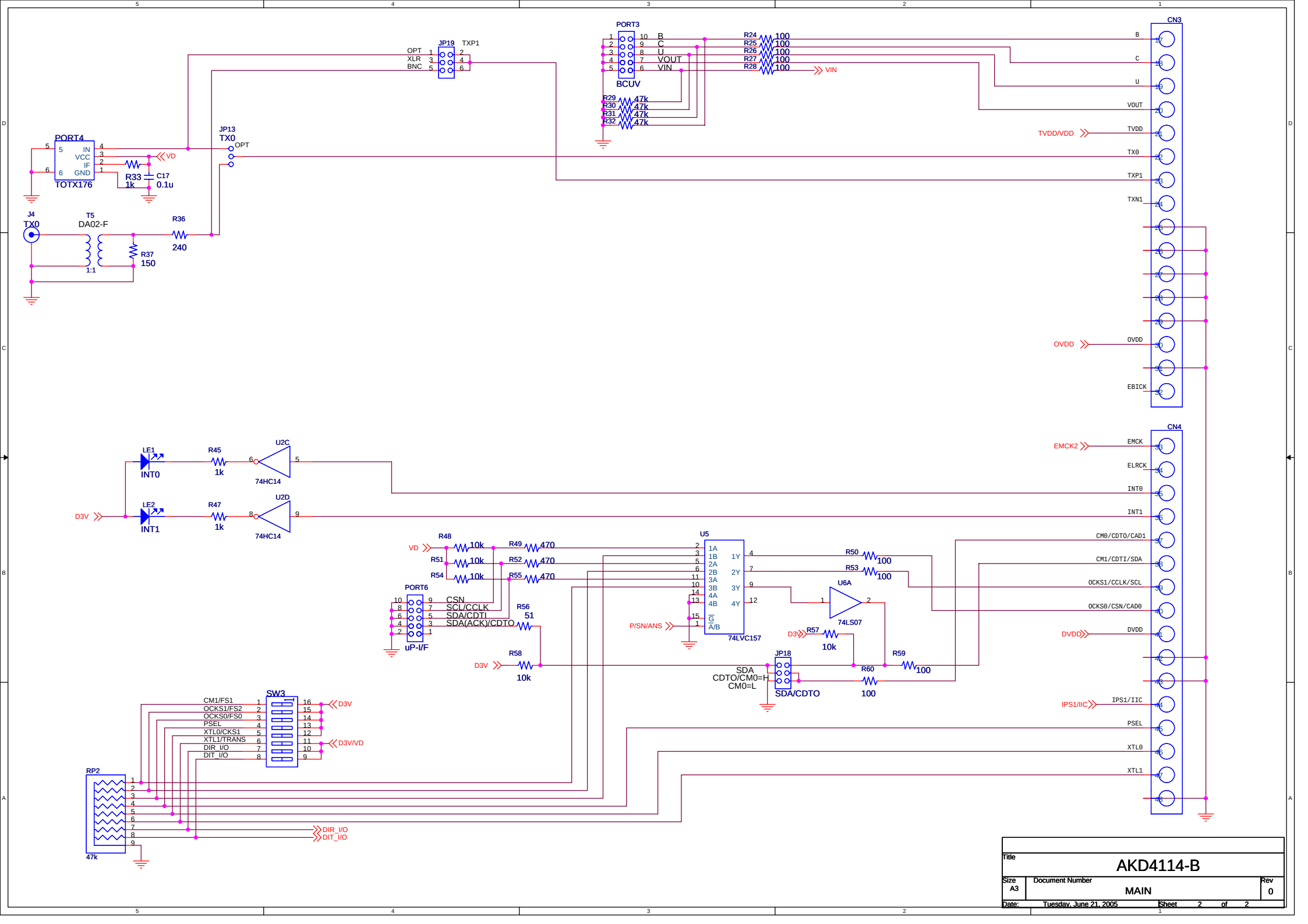
|---|---|---|
| Title | AKD4114-B | |
| Size A3 | Document Number MAIN | Rev 0 |
| Date: Friday, November 19, 2004 | Sheet 1 of 2 | |

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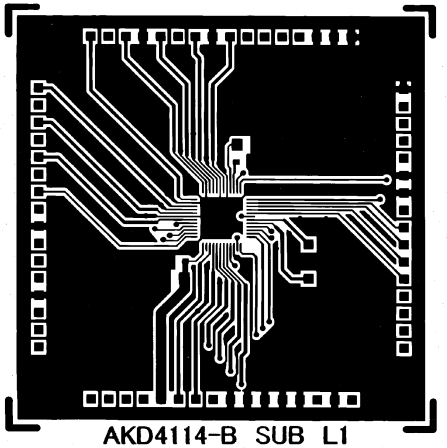
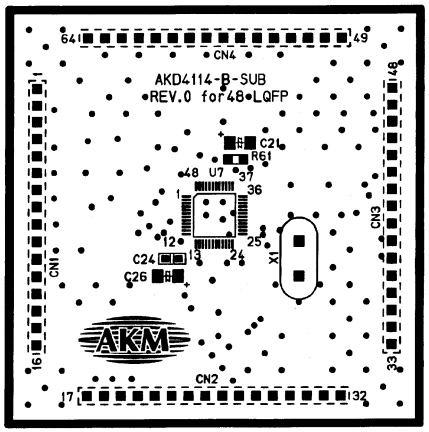
| Size A3 | Document Number MAIN | Rev 0 |
| Date: Tuesday, June 21, 2005 | Sheet 2 of 2 | |



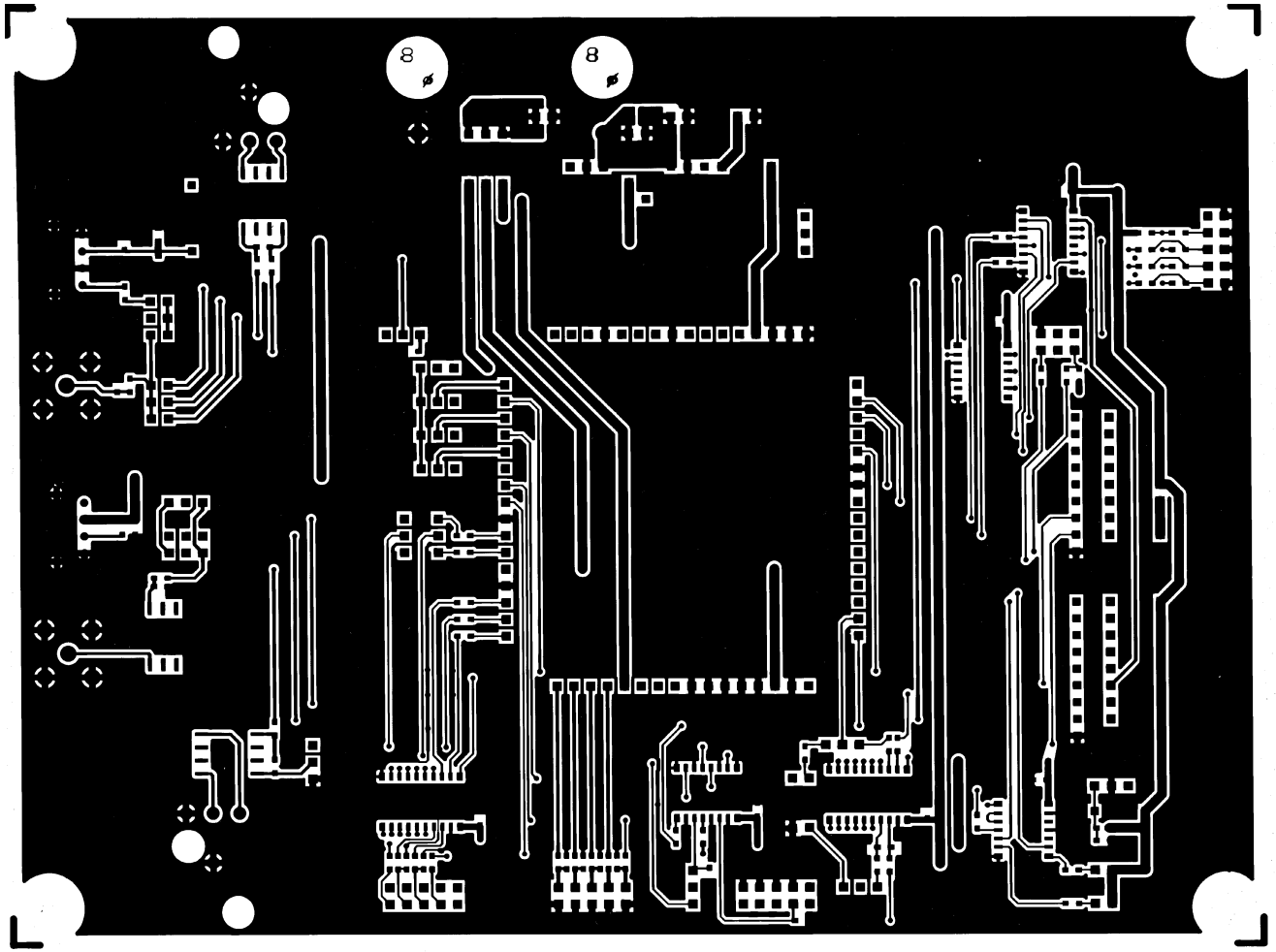
AKD4114-B SUB L1

AKD4114-B SUB L2

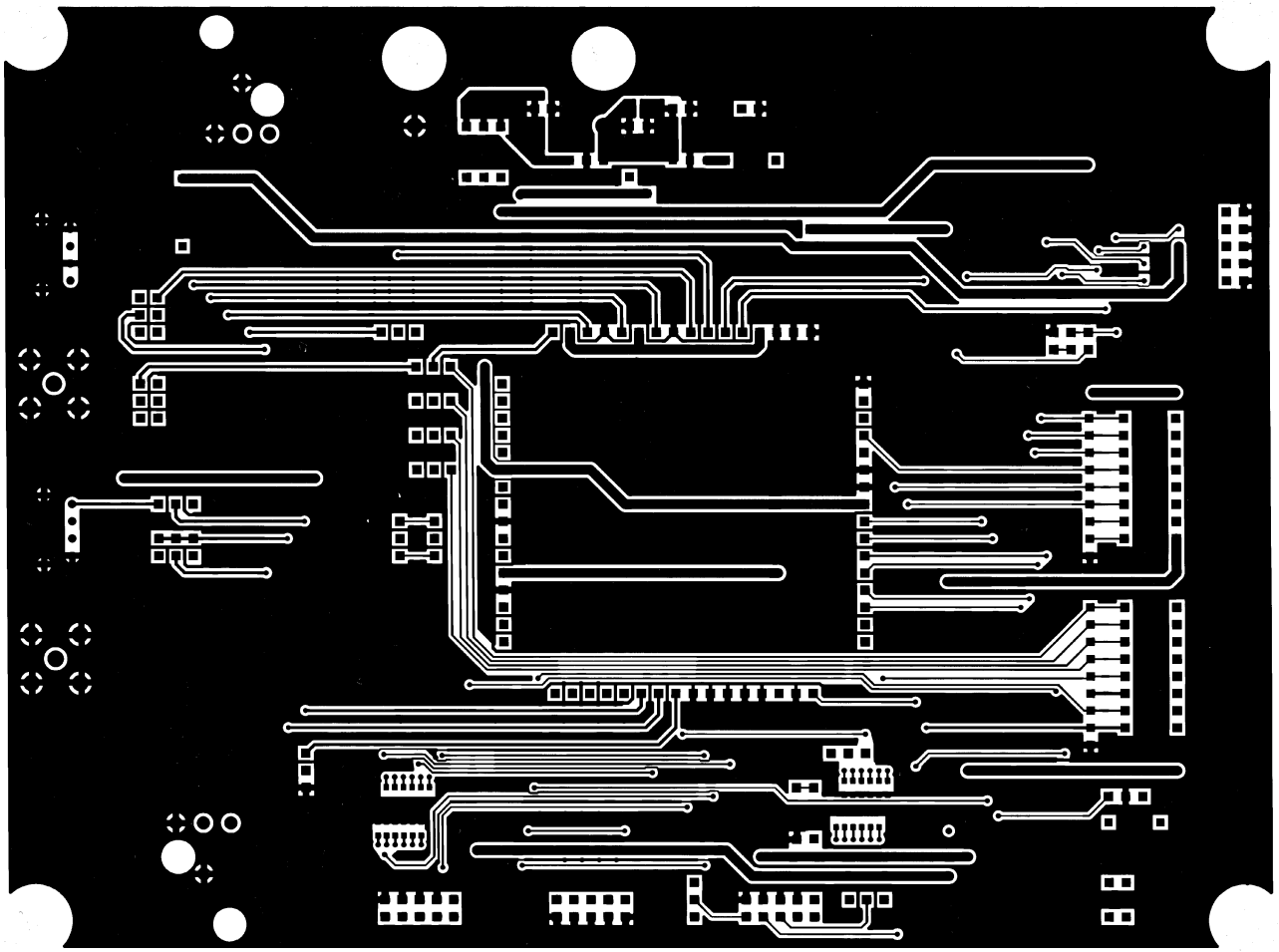



AKD4114-B SUB L1_SILK

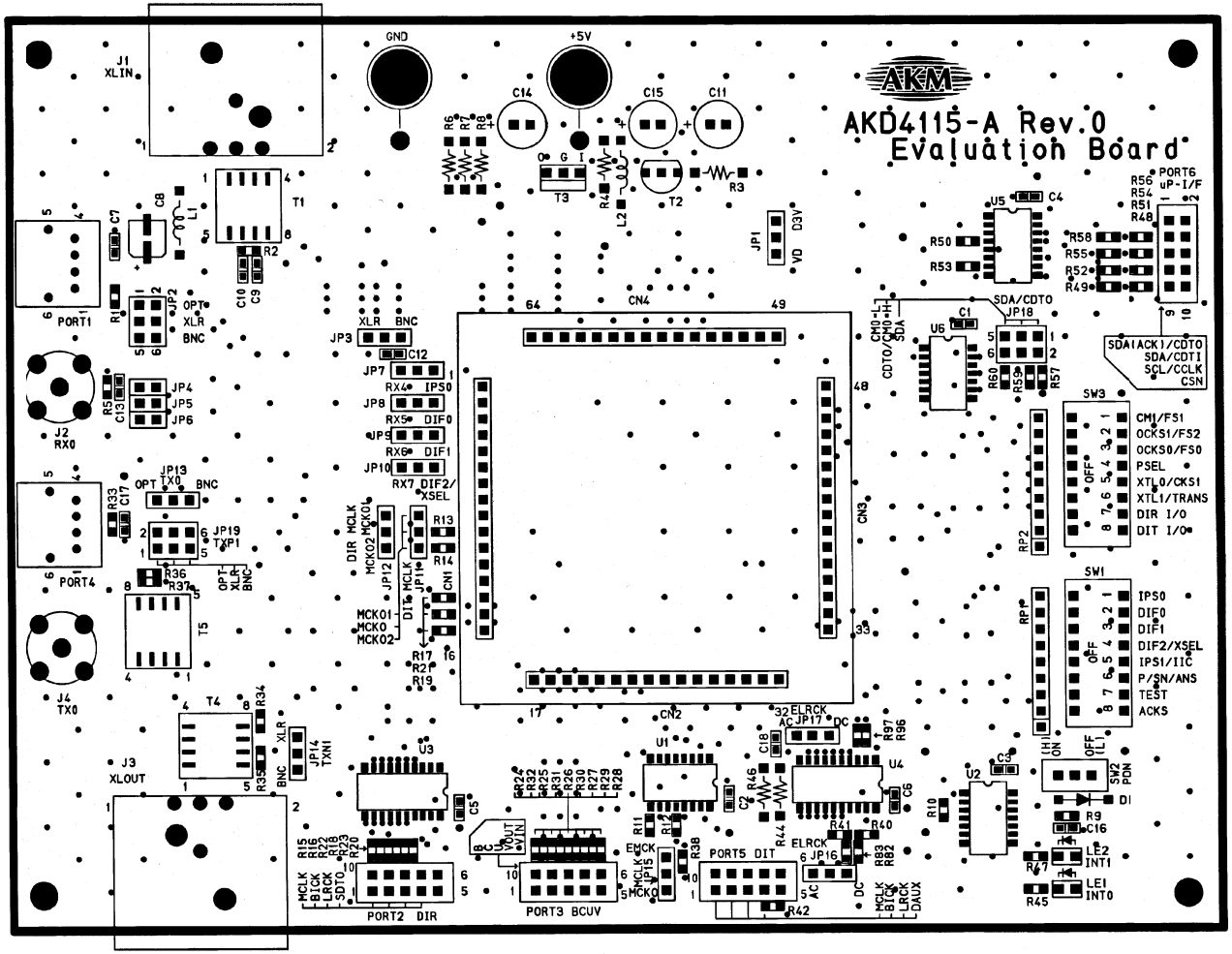
AKD4114-B SUB L2_SILK



AKD4115-A L1



AKD4115-A L2




AKD4115-A L1_SILK

AKD4115-A L2_SILK